Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in this application.

Listing of Claims:

Rule 1.126

Claims 1-~~12~~ 11 (Canceled)

~~13~~ 12. (New) A method of caching commands in microprocessors having a two- or multidimensional configurable cell arrangement, comprising:

combining a plurality of configurable cells to form a plurality of groups;

assigning a first cache unit to a first group;

connecting the first cache unit via a tree structure to a higher level cache unit having access to a command memory in which commands are stored;

combining commands to form command sequences;

caching the command sequences as a whole;

sending a request for a required command from the first cache unit to the higher level cache unit;

sending a first command sequence including the required command to the first cache unit if the higher level cache unit holds the first command sequence including the required command in the higher level cache unit's local memory; and

sending the request for the required command from the higher level cache unit to a respective higher level cache unit if the higher level cache unit does not hold the first command sequence including the required command in the higher level cache unit's local memory.